$\left\langle v_{1}^{b}\right\rangle$	1. A system interface comprising:					
<u>}</u>		(a)	a plura	ality of first dire	ector boards, each one of the first director boards having:	
3			(i)	a plurality of	first directors; and	
4			(ii)	a crossbar swi	tch having input/output ports coupled to the first	
5	directors on such one of the first director boards and a pair of output/input ports;					
6		(b)	a plura	ality of second	director boards, each one of the second directors boards	
7	having	:				
8			(i)	a plurality of	econd directors; and	
9			(ii)	a crossbar swi	tch having input/output ports coupled to the second	
10	directors on such one of the second director boards and a pair of output/input ports;					
11		(c)	a data	transfer section	having a cache memory, such cache memory being	
12	coupled to the plurality of first and second directors;					
13		(d)	a mess	sage network, o	perative independently of the data transfer section; and	
14		(e)	where	in the first and	second directors control data transfer between the first	
15	directors and the second directors in response to messages passing between the first directors					
16	and the second directors through the message network to facilitate data transfer between first					
17	directors and the second directors with such data passing through the cache memory in the					
18	data tra	ınsfer s	ection.			
1		2.	The sy	stem interface	ecited in claim 1 wherein each one of the first directors	
2	include	es:				
3	a data pipe coupled between an input of such one of the first directors and the cache					
4	memor	y;				
5	a controller for transferring the messages between the message network and such one of the					
6	first dir	ectors.				
1		3.	The sy	stem interface	recited in claim 1 wherein each one of the second	
2	directors includes:					
3	a data pipe coupled between an input of such one of the second directors and the					
4	cache n	nemory	/;			



a controller for transferring the messages between the message network and such one of the second directors.

4. The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

5. The system interface recited in claim 1 wherein each one of the first directors includes:

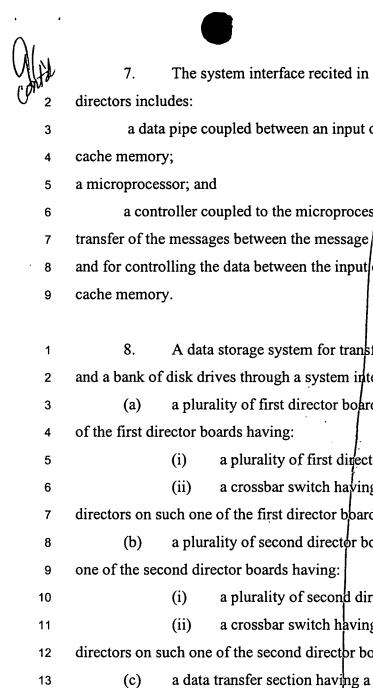
a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

- 6. The system interface recited in claim 1 wherein each one of the second directors includes:
- a data pipe coupled between an input of such one of the second directors and the cache memory;
- a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.



7.	The system interface recited in claim 5 wherein each one of the second						
directors includes:							
a data pipe coupled between an input of such one of the second directors and the							
cache memory;							
a microprocessor; and							
a controller coupled to the microprocessor and the data pipe for controlling the							
transfer of the messages between the message network and such one of the second directors							
and for controlling the data between the input of such one of the second directors and the							
cache memory.							
8.	A data storage system for transferring data between a host computer/server						
and a bank of disk drives through a system interface, such system interface comprising:							
(a)	a plurality of first director boards coupled to host computer/server; each one						
of the first dire	of the first director boards having:						
	(i) a plurality of first directors; and						
	(ii) a crossbar switch having input/output ports coupled to the first						
directors on su	directors on such one of the first director boards and a pair of output/input ports;						
(b)	a plurality of second director boards coupled to the bank of disk drives, each						
one of the second director boards having:							
	(i) a plurality of second directors; and						
	(ii) a crossbar switch having input/output ports coupled to the second						
directors on such one of the second director boards and a pair of output/input ports;							
(c)	a data transfer section having a cache memory, such cache memory being						
coupled to the plurality of first and second directors;							
(d)	a message network, operative independently of the data transfer section; and						
(e)	wherein the first and second directors control data transfer between the host						
computer and the bank of disk drives in response to messages passing between the first							
directors and the second directors through the message network to facilitate the data transfer							
between host computer/server and the bank of disk drives with such data passing through the							
cache memory in the data transfer section:							

